AMENDMENTS TO THE SPECIFICATION

Please amend Paragraph [09] as follows:

--Figs. 3A and 3B illustrate ~~illustrates~~ a method of forming an electrical component on a material for a wearable item according to an embodiment of the invention.--.

Please amend Paragraph [15] as follows:

--Fig. 2 illustrates an enlargement and cross section of a portion of the warp fiber 103A having an electrical component 107 (along line I – I' in Fig. 1). In particular, this figure illustrates a cross-section of one portion of the warp fiber 103A that has a NPN bipolar junction transistor 201 formed thereon. The structure of this transistor 201 will be discussed in detail below with reference to Fig. 2. Further, a method of forming the transistor 201 according to the invention will be discussed with reference to Figs. 3A and 3B.--.

Please amend Paragraph [16] as follows:

--Referring now to Fig. 3A, in step 301, a substrate 203 is formed on the surface 205 of the fiber 103A. As seen in Fig. 2, the substrate 203 forms a base on the fiber 103A to support the transistor 201. The substrate 203 may be formed of any suitable material, including those materials typically used as a substrate in the conventional manufacture of conventional integrated circuits, such as metals, plastics, glasses, composite materials, and ceramics. In the particular embodiment illustrated in Fig. 2, the substrate 203 covers only a portion of the circumference of the fiber 103A. It should be noted, however, that with alternate embodiments of the invention, the substrate 203 may encompass the entirety of the circumference of the fiber 103A. While providing a substrate 203 that only partially covers the circumference of the fiber 103A better allows the fiber 103A to retain its native properties (*e.g.*, flexibility, appearance), covering the entire circumference of the fiber 103A may be useful in order to better adhere the substrate 203 to the surface 205 of the fiber 103A.--.

Please amend Paragraph [17] as follows:

--The use of the substrate 203 may provide a number of desirable advantages. First, the substrate 203 may be formed of a material that will provide a strong adherence of the transistor 201 to the fiber 103A. Moreover, the substrate 203 may be formed to provide a smooth surface upon which the transistor ~~21~~ 201 can be deposited. This use of the substrate 203 to provide a smooth surface may be particularly beneficial where, *e.g.*, the fiber 103A has an uneven or rough surface, such as commonly found with natural fibers. It should be noted, however, that for alternate embodiments of the invention, the substrate 203 may be omitted entirely. For example, where the material employed to form the bottom structure of the transistor 201 will strongly adhere to the surface of the fiber 103A, and the surface of the fiber 103A is sufficiently smooth to form the transistor 201 thereon, then the substrate 203 may be omitted.--.

Please amend Paragraph [18] as follows:

--Next, in step 303, a layer 207 of *p*-type substrate material is formed on the surface of the substrate 203. The layer 207 may be formed of any suitable material employed for conventional transistor fabrication, such as silicon. Further, the layer 207 of *p*-type substrate material may be doped as necessary for the transistor 201 to have the desired operating parameters.--.

Please amend Paragraph [21] as follows:

--As will be appreciated by those of ordinary skill in the art, the Miller et al. techniques can be used to form the layer 207 of material that has already been doped to ~~posses~~ possess the desired *p*-type characteristics. Alternately, the Miller et al. techniques can be used to form the layer 207 of undoped material. The layer 207 can then subsequently be doped to have the desired *p*-type characteristics using a suitable conventional doping technique, such as ion implantation or diffusion.--.

Please amend Paragraph [22] as follows:

--In step 305, an n^+-type region 209 is formed in the layer 207. Again, the n^+-type region can be formed using any suitable conventional doping technique, such as ion implantation or diffusion. Next, ~~in step 307,~~ a layer 211 of n-type material is deposited over the layer 207 of p-type material. As with the formation of the layer 207 of p-type material, the Miller et al. techniques can be used to form the layer 211 of p-type material that has already been doped to ~~posses~~ possess the desired p-type characteristics. Alternately, the Miller et al. techniques can be used to form the layer 211 of undoped material, which can be doped to have the desired n-type characteristics using a suitable conventional doping technique, such as ion implantation or diffusion.--.

Please amend Paragraph [23] as follows:

--Next, in step 307, two p^+-type regions 213A and 213B are formed in the layer 211, in order to isolate an n-type region 215 in the layer 211. Then, in step 309, a p-type region 217 is formed within the n-type region 215, in order to create a base for the transistor 201. Subsequently, in step 311 (see Fig. 3B), an n^+-type region 219 is formed in n-type region 215 and an n^+-type region 221 is formed in p-type region 217, to create a collector and emitter, respectively, for the transistor 201. As previously noted, each of the doped regions 213A, 213B, 215, 217, 219 and 221 can be created using any suitable conventional doping technique, such as ion implantation or diffusion. Of course, n^+-type regions 219 and 221 may alternately be formed in different steps.--.

Please amend Paragraph [24] as follows:

--In step 313, the electrodes 223A, 223B and 223C are formed to provide the collector electrode, the base electrode, and the emitter electrode, respectively. The electrodes 223A, 223B and 223C can conveniently be formed using the techniques described in the Miller et al. patent referenced above. As will be appreciated by those of ordinary skill in the art, the electrodes 223A, 223B and 223C can be formed as part of

connection lines 109, or they can be formed as individual contacts and then subsequently connected to connection lines 109.--.

Please amend Paragraph [29] as follows:

--While the above-described example relates to the formation of a bipolar junction transistor onto a fiber, those of ordinary skill in the art, upon reviewing this application, will appreciate that the teachings of the invention encompass forming a variety of electrical components onto a fiber. For example, as shown in Fig. 4, the technique disclosed in the Miller et al. patent can be used according to the invention to form a patterned line 403 on the fiber 401. Via a connection line 109, the patterned line 403 can be connected to other electrical components ~~109~~ 107 that form an electrical device (not shown), so that the patterned line 403 acts as an antenna element for the electrical device. Still, further, the Miller et al. technique (or other suitable technique) can be used to form a layer of resistive material sandwiched between two layers of conductive material, to thereby form a capacitor. Thus, those of ordinary skill in the art will understand that, according to the teachings of the invention, any structure that can be fabricated using the Miller et al. technique or other suitable technique can be formed on a fiber in such a way that the fiber may be subsequently woven into a fabric for, *e.g.*, clothing or other articles of wear.--.